CLAIMS

1. An On-Screen-Display (OSD) insert circuit comprising:

an OSD signal generator for generating a switching signal and an analog additional image signal based on a first clock signal;

an analog-to-digital converter for converting the generated additional image signal into a digital additional image signal based on a second clock signal as a sampling clock signal;

a switching circuit for switching between a digital video signal and the digital additional image signal based on the switching signal as to selectively output the digital video signal and the digital additional image signal; and

a control-signal generator, wherein the digital video signal has a horizontal synchronizing signal, the control-signal generator being operable to

reset the first clock signal with a signal having a predetermined phase difference including zero with reference to the horizontal synchronizing signal, and

generate the second clock signal so that a phase of the second clock signal is adjusted with respect to the horizontal synchronizing signal.

2. The OSD insert circuit of claim 1, further comprising:

a time-division-multiplexing circuit for time-multiplexing the switching signal and the digital additional image signal based on a third clock signal; and

a decoder for decoding the time-multiplexed switching signal and the time-multiplexed additional image signal,

wherein the switching circuit switches, based on the decoded switching signal, between the digital video signal and the decoded additional image signal as to selectively output the digital video signal and the decoded additional image signal, and

wherein the control-signal generator is operable to generate the third clock signal.

3. The OSD insert circuit of claim 2,

wherein the digital video signal further has a fourth clock signal,

wherein the control-signal generator is operable to generate the third clock signal by multiplying a frequency of the fourth clock signal.

4. The OSD insert circuit of claim 3, wherein the control-signal generator is operable to adjust the phase of the second clock signal based on the third clock signal.

5. The OSD insert circuit of claim 4, wherein the control-signal generator is operable to generate the second clock signal by frequency-dividing the fourth clock signal.

6. The OSD insert circuit of claim 5, wherein a frequency ratio of the third clock signal to the fourth clock signal is different from a frequency ratio of the second clock signal to the fourth clock signal.

7. The OSD insert circuit of claim 6, wherein the control-signal generator is operable to

generate the third clock signal by multiplying the frequency of the

fourth clock signal by two, and

generate the second clock signal by dividing the frequency of the fourth clock signal by four.